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EXAMINER	
VIDWAN, JASJIT S	
ART UNIT	PAPER NUMBER
2182	
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11/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,419	GEHMAN ET AL.	
	Examiner	Art Unit	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *8-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 & 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are pending.

Claims 8-15 have been withdrawn from consideration as per response filed on 3/14/07.

Therefore, Claims 1-7 & 16-20 is being considered in this office action.

Applicant is respectfully advised to cancel any non-pending claims.

Response to Arguments

1. Applicant's arguments filed 08/30/07 have been fully considered but they are not persuasive. Applicant argues that prior art of record fails to teach:

(a) "Device hardware abstraction layer" - Applicant argues that the claimed limitation is in the software alone and is not getting mapped to hardware as is done by Bowen. Further Applicant argues that Bowen does not disclose abstraction layer that defines offset values for registers of a peripheral device or a data structure for the peripheral device

(b) "Platform hardware abstraction layer" – Bowen does not disclose platform hardware abstraction layer that defines an address map and further is adapted to initialize each instantiation of the peripheral device via calls to the device hardware abstraction layer

(c) "Abstraction layer adapted to initialize each instantiation of the peripheral device via calls to the device hardware abstraction layer and further wherein the device hardware abstraction layer has configurable memory register locations that are configured by the platform abstraction layer." Applicant also contests that Bowen does not teach abstraction layer having an interrupt configuration.

2. With respect to argument (a), **Examiner disagrees**. To the extent of Applicant's arguments in both (a) & (b) above with regards to software being mapped to hardware which is apparently contrary to Applicant invention, the argument is irrelevant as is no portion of the currently claimed invention indicates such limitation. Remaining true to the Applicant's actual invention, Bowen teaches a reusable software system wherein for a particular hardware

(controller for peripheral or any other hardware capable of running the said software block), a "behavioral synthesis" [see Paragraph 0053] is performed. Behavioral synthesis allows partition of software block that is capable of simply performing a "type of function" per se on the said hardware system. This software block with its behavioral synthesis can be run on any type of processor in the market. The second portion of the platform is the "RTL synthesis" (comparable to Applicant's platform hardware abstraction layer which is specific to a given peripheral or task) which optimizes the hardware description as attained from the behavioral synthesis and maps it to a given technology [see Paragraph 0145]. Therefore, it is the position of the Examiner that although the terminology might not match word for word, the substance of the invention can be paralleled in Bowen as indicated above.

3. With respect to argument (b), **Examiner disagrees**. Applicant argues that prior art fails to teach platform hardware abstraction layer that defines an address map of a system and particularly for the multiple instantiations of a peripheral device. Bowen teaches a system wherein the said software block is being run on a processor of a given hardware and thus as software block which provides an address map and in addition defines register values for the said register set as was also argued above **[see Paragraph 0173]**.

4. With respect to argument (c), **Examiner disagrees**. As was mentioned in above cited passage, Bowen teaches that one of the first functions of the said processor during startup/initialization is to define the memory register set and therefore it is suggested that the said function would occur during initialization **[see Bowen, Paragraph 0173]**. Furthermore, Applicant simply states that Bowen does not disclose an interrupt function, however this limitation was properly addressed during initial office action wherein Bowen taught the size of internal memory and of the stack or stacks can be set, the number and priorities of interrupts can be defined, an channels needed to communicate with external resources. **[See Page 8, Paragraph 0170].**

5. Therefore in light of above response, it is the position of the Examiner that prior art of record still reads on the claimed invention and thus the action is made FINAL.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7 & 16-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Bowen, U.S. Publication No: 200/0100029 **[herein after Bowen]**.

3. **As per Claims 1 & 16**, Bowen teaches a system for instantiating multiple instances of a peripheral device within an integrated circuit using a single configurable code block **[see Page 12, Paragraph 0241-- *Bowen teaches a system of using the single code block coupled with a hardware tailored for a specific peripheral device to simply 'share' the block to allow using the dedicated software with greater flexibility for multiple functionality. This method of coding overcomes similar shortcoming of Applicant's prior art wherein the software block has to be reconfigured repeatedly [see Bowen, paragraph 0005] to use with a separate hardware device as is discussed in Applicant's "Background of the Invention"*]**, the system comprising:

> (a) Device hardware abstraction layer **[see Fig. 2, element 212, "Behavioral Synthesis"]** defining a configurable structure **[see Page 3, Paragraph 0053, "Behavioral description of the electronic system" – also see paragraph 0038]** for the peripheral device **[see Fig. 10, elements 1024, 1026, 1028, 1032, etc – also see Page 12, Paragraph 0238 for full list of peripheral devices]**
>
> (b) Platform hardware abstraction layer **[see Fig. 2, element 214, RTL Synthesis]** adapted to configure the structure of each particular instantiation of the peripheral device via the device hardware abstraction layer **[see Page 7, Paragraphs 0144 & 0145 – "RTL synthesis optimizes the hardware description and <u>maps it to a given technology</u>.]**.

4. **As per Claim 2 & 17**, Bowen teaches a system wherein the device hardware abstraction layer comprises:

(a) Memory registers location **[see Paragraph 0054]** adapted to the configurable during initialization of the system **[see Paragraph 0173]**

(b) Interrupt configuration, which is configured for the peripheral device during initialization of the system **[see Page 8, Paragraph 0170 – "The size of internal memory and of the stack or stacks can be set, the number and priorities of interrupts can be defined, an channels needed to communicate with external resources.."]**

5. **As per Claim 3 & 18**, Bowen teaches a system wherein the memory register locations and the interrupt configurations define the structure of the peripheral device using variables **[see Paragraph 0062, "Variables are declared with explicit bit widths and the operators working on the variables work with an arbitrary precision."]**

6. **As per Claim 4, 5 & 19**, Bowen teaches a system wherein the platform hardware abstraction layer comprises a memory map of memory locations of the peripheral device corresponding to a particular implementation of the peripheral device, the memory map adapted to replace the variables with unique memory locations for each instantiation **[see Paragraph 0315 – "Look up table (LUT)" with "resources" being the peripheral devices]**.

7. **As per Claim 6, 7 & 20**, Bowen teaches a system wherein the configurable structure of the peripheral device is defined in the device hardware abstraction layer using variables, the platform hardware abstraction layer comprising an interrupt configuration corresponding to interrupt connections for a particular implementation of the peripheral device, the interrupt configuration adapted to replace the variables with unique interrupt connections for each instantiation **[see Paragraph 0306]**.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
11/13/07

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SUPERVISORY PATENT EXAMINER